Microwind delay evaluation

DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the ...

Microwind 3.1 includes the ability to evaluate delay globally for each interconnect using simple analytical approximations. The delay is calculated as a function of the resistance and capacitance of the ...

The module functionality and performance issues like area, power dissipation and propagation delay are analyzed at 0.12µm 6metal layer CMOS technology using microwind tool.

The circuit of the six different power and delay reduction techniques of full adder with XOR gate designed by using MICROWIND tool and its layout be generated with the help Microwind EDA editor ...

Introducing 14-nm FinFET technology in Microwind This paper describes the implementation of a high performance FinFET-based 14-nm CMOS Technology in Microwind. New concepts related to the ...

In this thesis proposed a reduction of delay, leakage current, leakage power. First find out the leakage current and leakage power. This thesis uses a gate diffusion input technique.

Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D ...

Click "Analysis" "Global Delay Evaluation" within microwind to access to this command.

- Improved Global Delay Evaluation at integrated circuit level. - Enhanced Global Crosstalk evaluation effect based on analytical approximations of the coupling amplitude. - Improved and new Help on ...

Is there a way to measure rise/fall time, 10%-90% in Microwind? What is shown is the 50% propagation delay I presume.

Web: https://rocksteadyfloors.co.za